Summary of Japanese Patent Publication No. 2002-198802 (non-examined)

Publication number: 2002-198802
Date of publication of application: 12.07.2002
Application number: 2000-398585
Applicant: ANDO ELECTRIC CO LTD
Date of filing: Dec. 27, 2000
Inventor: Masayuki TAKAHASHI

Title: PLL CIRCUIT AND METHOD FOR CONTROLLING THEREFOR

This invention is for measuring jitters of a phase lock loop circuit.

A jitter measurement apparatus 20, such as an oscilloscope as shown in Fig. 4b, has been used to measure jitters of the output signal of a phase lock loop circuit 10 as shown in Fig. 4a.

If the carrier to noise (C/N) characteristic of a reference signal is worse than that of a VCO 13, jitter of the reference signal affects the output signal under test. Especially, it is considerable if another PLL circuit produces the reference signal, which leads to more jitter measured than the actual one in the output signal.

Fig. 4 (a)

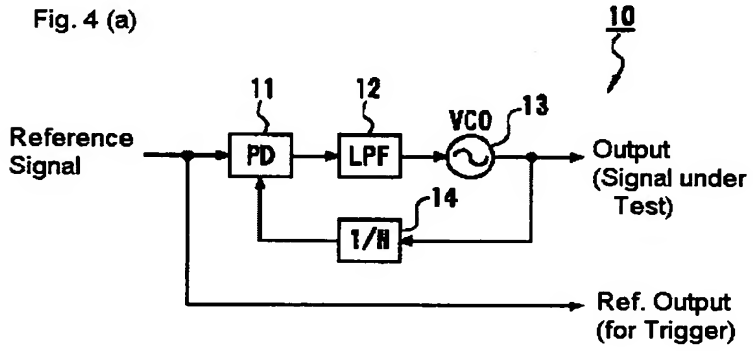
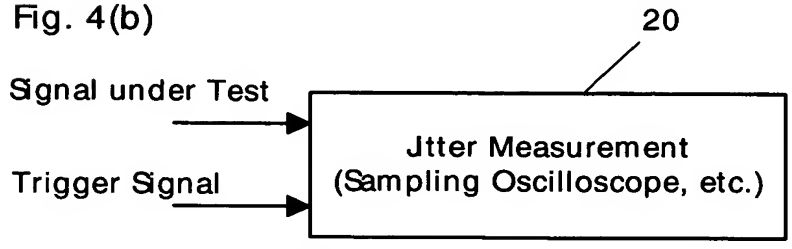


Fig. 4(b)



Frequency of Signal under test = Trigger Signal x N

* "N" is an integer.

Then, this invention provides a more accurate jitter measurement than before. Referring to Fig.1, this invention provides a switch 105 to select a signal having a better C/N characteristic from an N divided signal and a reference signal 2 according to a switch control signal. Therefore, the jitter of the output signal is measured according to a less jittered trigger signal.

Fig. 1